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EXAMINER	
BOLOURCHI, NADER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,898	NELSON ET AL.	
	Examiner	Art Unit	
	Nader Bolourchi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/19/2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7,10-15,17,18,20 and 21 is/are rejected.

7)☒ Claim(s) 8 and 9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicant's amendment dated 3/19/2007 is entered.

2. Applicant canceling claims 16 and 19 is acknowledged.

3. Claims stand objected.

4. Claim Rejections under 35 USC § 112, first paragraph, is withdrawn.

5. Claims stand rejected under 35 USC § 103.

6. All amended claims are rejected under 35 USC § 103.

Response to Arguments

7. Applicant's arguments filed 3/19/2007 have been fully considered but they are not persuasive.

8. The Applicants argues as follow (emphasis added):

> It is known to use fractional re-sampling in multi-rate systems. When used in a demodulator (the receive end of a communication, as opposed to a modulator at the transmit end of the communication), use of digital timing error correction has also been introduced as part of digital modems. This timing error correction refers to symbol timing synchronization that must be implemented as part of the demodulator. Mueller concerns fractional interpolation at the modulator. Gardner (the inventor, not necessarily the cited reference) is recognized as a key researcher in the field of fractional interpolation at the demodulator. The Examiner relies upon Gardner's timing error detector 106 at the demodulator as relevant to the timing error detector sub-circuit of claim 1 and the detector loop of claim 18.

Examiner respectfully disagrees. Mueller clearly shows use of Fractional Interpolator (means 54) in both transmitter (Fig. 6) and receiver (Fig. 5). Examiner notes that Applicant is responsible for understanding the reference in its entirety.

Furthermore, Applicant properly notes that (emphasis added)

> As seen in Figure 2, embodiments of this invention are detailed with respect to the transmit side of a communication, the modulator. In both this invention and Mueller, fractional re-sampling is implemented at the modulator by decoupling the symbol-rate clock from the digital-to-analog converter (DAC) sampling clock.

However, as stated earlier, Mueller uses the Fractional Interpolator both in transmitter and receiving end.

Applicant further argues that (emphasis added):

> side of a communication, the modulator. In both this invention and Mueller, fractional re-sampling is implemented at the modulator by decoupling the symbol-rate clock from the digital-to-analog converter (DAC) sampling clock. This can be thought of as asynchronous sampling since the symbol-rate clock and the DAC sample-rate clock are not related by an integer factor, though in truth these clocks must be synchronized by some digital means. Generically term this some kind of a digital symbol-rate (and data-rate) synchronization circuit. This allows crossing the boundary from the symbol-rate clock domain to the sample-rate clock domain. It is this boundary crossing that is fundamentally different as between the modulator and the demodulator side of a communication, and the clearest distinction over Gardner and Harnden.

Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. , It is noted that

the features upon which applicant relies (i.e., **underlined**) are not recited in the rejected claim(s).

Applicant also argues that (emphasis added):

> The Office Action recites that it would be obvious to include a timing error detector as taught in Gardner in the re-sampling circuit of Mueller. This may be true for those teachings of Mueller related to demodulation, but are inapposite for Mueller's teachings related to fractional interpolation at the modulating side of a communication.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Applicant also argues (emphasis added):

> Regardless, Gardner's timing error detector 106 is seen to have a single input, the strobes Z(m) from the interpolator 120 that are used to correct phase in the VCO 112 (sample timing). Claim 1 recites that the timing error detector sub-circuit has two inputs: one from a symbol rate clock and the other from a strobe.

Examiner respectfully disagrees. Z (m) is not a single input. Furthermore, 106 is used to aligning strobes Z (m) with the ideal signal levels (other input), which is estimated value (see column 5: lines 33-50; equations 5.1-3). For example, in case of partial response, recovery of an individual symbol value generally requires that information be combined from several strobes (see column 3: lines 51-65).

Applicant also argues:

> The Office Action does not appear to address the parallel implementation recited in claim 1, which recites in relevant part:
>
> an oscillator having...N timing signal outputs for outputting N timing signals in parallel...
>
> at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel...
>
> This recites a *parallel* implementation of a modulator in which the sample-rate clock is decoupled from the symbol-rate clock (claim 1 recites the oscillator separately from the symbol rate clock).. Mueller is not seen to disclose, teach or suggest such a parallel implementation though the office action asserts otherwise in the detailed action at page 3. Such a modification to Mueller is not obvious, and still remains a technical challenge for high-data-rate software-defined radio systems. Even if multiple ones of the claimed "at least one fractional interpolator" were used in a modification to Mueller's teaching so that a series of single-input interpolators were arranged in parallel with one another, the claimed oscillator still has N timing signal outputs for outputting N timing signals in parallel. Mueller has no such parallel implementation.

It is not clear why applicant make above statement. The specification in page 3, lines 25-26, clearly defines N, as an integer greater than or equal one, which is also recited in claim 1. Examiner in all references used assumed N=1. Most or remainder of the Applicant's argument is a bout integer N. When N=1, there is no parallel entity.

Applicant also argues that,

> Assuming that Herndon's polyphase filter 600 can be reasonably interpreted as representing a serial to parallel converter that might be implemented in a transmitter (not admitted) and regardless of cyclic independence of sample and output rates, the mere combination of such a serial to parallel converter with Mueller's serial implementation cannot achieve "a numerically controlled oscillator NCO having a plurality of N outputs coupled to respective N inputs of the fractional interpolator for providing N timing signals for respective ones of the interpolated data points" as recited in amended claim 20. Claim 20 is seen to distinguish over the cited combination, which like Gardner and Mueller, is seen to be improper for the modulation side of a communication.

Applicant provide no reason in support of above statement, except for what already discussed, i.e., Mueller clearly shows use of Fractional Interpolator (means 54) in both transmitter (Fig. 6) and receiver (Fig. 5).

Therefore, claims 1-7, 10-15, 17-18, and 20-21 stand rejected.

Claim Objections

9. Claim 5 is objected to because of the following informalities: The claim recites the limitation "fractional interpolator filter" in line 1. There is insufficient antecedent basis for this limitation in the claim. Examiner suggests removal of phrase "filter" from the limitation.

Claims 8, 13, 17, 18, and 20; recites "N" which is not defined. Examiner suggests adding phrase: "wherein N is an integer greater than or equal to one", recited in claim 1, to these claim, as per lines 25-26, page 3 of the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 7, 10, 11, and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller (US Pub 2003/020.4542) in view of Gardner et al. (US 5,805,619).

Regarding claim 1: Mueller discloses numerically controlled oscillator (Fig. 5: 60; Fig. 6: 60) having an input coupled to an output of the timing error-detector sub-circuit and N timing signal outputs for outputting N timing signals in parallel and a second output for outputting the strobe (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4); and one fractional interpolator having parallel inputs coupled to N data inputs in parallel and to the N timing signals in parallel, for outputting N data outputs in parallel, wherein N is an integer greater than or equal to one (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2). Mueller does not disclose a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe.

Gardner et al. disclose a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe (Column 2 Line 59 to Column 3 Line 5). It is clearly obvious to one of ordinary skill in the art that a timing error detector is desirable in a circuit for re-sampling N data inputs. A timing error detector allows for the measurement of the timing error in a strobe (See Gardner et al., Column 2 Lines 63-66) and that in turn allows for error correction. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a timing error detector in the re-sampling circuit of Mueller, as Gardner et al. teaches, in

order to allow for error correction.

Regarding claim 7: Mueller and Gardner et al. as stated in rejection of claim 1 above. Furthermore, Gardner et al. disclose, wherein the error detector sub-circuit operates to synchronize the strobe (Column 2 Lines 63-66 and Column 5 Lines 34-36).

Although Mueller and Gardner et al. do not explicitly disclose that the error detector sub-circuit operates to synchronize the strobe to a positive edge of the input that is coupled to the symbol rate clock, such limitation is merely a matter of design choice and would have been obvious in the system of Mueller or Gardner et al. The choice of synchronization of the strobe to a positive or negative edge is dependent upon the type of the input.

Regarding claim 10: Mueller and Gardner et al. as stated in rejection of claim 7 above. Furthermore, Gardner et al. disclose that the error detector sub-circuit synchronizes the strobe by adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, "aligning the sampling strobe timing" and "data signal is strobed (sampled) at properly timed intervals T" is interpreted as "adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock").

Regarding claim 11: Mueller and Gardner et al. as stated in rejection of claim 7 above.

Furthermore, Gardner et al. disclose that the error detector sub-circuit further comprises an oscillator data clock having an input coupled to the strobe, and an integrator having a first input coupled to an output of the oscillator data clock and a second input coupled to an output of the symbol rate clock, the integrator having an output coupled to an inverter, and wherein the oscillator input is coupled to an output of the inverter (Column 2 Lines 63-67 and Column 22 Lines 42-44, wherein, block 371 in Fig. 20 is interpreted as the inverter).

Regarding claim 13: Mueller discloses synchronizing a local clock to a symbol clock (Paragraph 0034 Lines 11-13); determining a plurality of n parallel timing signals based on the synchronized local clock (Paragraph 0005 Lines 12-13 and Lines 20-22; Examiner notes that N=1); providing the N parallel timing signal and a strobe from the local clock to an interpolating filter (Paragraph 0006 Lines 1-9; Examiner notes that N=1); providing a timing feedback to synchronize the local clock to the symbol clock (Paragraph 0005 Lines 16-20). Mueller does not teach, re-sampling a data sample input at a time within a symbol period determined by the timing signal and the strobe.

However, as discussed in claim 10 above, Gardner et al. teaches, re-sampling a data sample input at a time within a symbol period determined by the timing signal and the strobe (Column 8 Lines 16-19 and Column 5 Lines 11-13, Local clock 112 in Fig. 2; wherein, "coincide with the instants of ideal signal levels" is interpreted as "the time

within a symbol period").

Regarding claim 14: Mueller and Gardner et al. as stated in rejection of claim 13 above. Furthermore, Gardner et al. teach that synchronizing a local clock to a symbol clock comprises determining a difference between the symbol rate clock signal and one of at least two data strobes and providing a frequency adjustment output based on the difference (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, 'output error control signal' is interpreted, as providing a frequency adjustment output).

Regarding claim 15: Mueller and Gardner et al. as stated in rejection of claim 13 above. Furthermore Gardner et al. teach that the timing feedback comprises a most significant bit of an amplified frequency signal accumulated in a register (Column 3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the most significant bit of an amplified frequency signal accumulated in a register).

Regarding claim 17: Mueller teaches inputting a symbol rate and a data strobe (Paragraph 0024 Lines 1-7).

As discussed in claim 10, Gardner et al. teaches: measuring a difference between the data strobe and the symbol rate (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, "output error control signal" is interpreted as "the difference between the data strobe and the symbol rate"); adjusting a next data strobe to match the symbol rate

(Column 8 Lines 16-19, wherein, "aligning" is interpreted as "adjusting"); determining a plurality of N timing signal based on the difference (Column 8 Lines 16-19, wherein, "output error control signal" is interpreted as "the timing signal"); and fractionally re-sampling in parallel a plurality of N data sample at a time within a symbol period defined by individual ones of the plurality of N timing signal (Column 5 Lines 11-13; Examiner notes that N=1).

Regarding claim 18: Mueller discloses a numerically controlled oscillator NCO having an input coupled to the frequency adjustment output, and for outputting the data strobe and a plurality of N timing signal in parallel (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4; Examiner Notes that N=1); and a fractional interpolator having a plurality of N parallel data inputs coupled to N data sample inputs, a first timing input coupled to the data strobe, and a plurality of N second timing inputs coupled to individual ones of the N timing signals, for re-sampling in parallel the N data sample inputs at a time within a symbol period defined by the individual ones of the timing signal (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2; Examiner notes that N=1). Mueller does not disclose, a detector loop having an input coupled to an output of a symbol rate clock signal and to a data strobe, for determining a difference there between, and for providing a frequency adjustment output based on said difference.

However, as discussed in claim 1 above, Gardner et al. discloses, a detector loop having an input coupled to an output of a symbol rate clock signal and to a data strobe,

for determining a difference there between, and for providing a frequency adjustment output based on said difference (Column 2 Line 59 to Column 3 Line 5, Column 8 Lines 16-19, and Column 5 Lines 11-13, wherein, "output error control signal" is interpreted as "the difference between the symbol rate clock signal and the data strobe").

11. Claims 2, 3, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller and Gardner et al. and further in view of Boerstler (US 6,353,369).

Regarding claim 2: Mueller and Gardner et al. as stated in rejection of claim 1 above. Mueller or Gardner et al. do not disclose that the oscillator comprises a plurality of N amplifiers each defining a different gain.

However, Boerstler discloses that the oscillator comprises a plurality of N amplifiers each defining a different gain (Column 2 Lines 51-56, wherein, the integer seven is interpreted as N). It is fundamental that a NCO comprises a plurality of N amplifiers each defining a different gain. Different amplifier gains allow for the production of various voltage levels at the amplifiers outputs, i.e., allow for the production of various voltage levels to be coupled to the oscillator. Various voltage levels coupled to the oscillator, in turn, allow for the production of greater number of possible NCO output states. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the NCO of Mueller and Gardner et al. a

plurality of N amplifiers each defining a different gain, as Boerstler teaches, in order to increase the number of possible NCO output states.

Regarding; wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers, and wherein N is an integer greater than one, Gardner et al. further discloses, wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers, and wherein N is an integer greater than one (Column 3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the most significant bit selected from an output of one of the amplifiers).

Regarding claim 3: Mueller, Gardner et al. and Boerstler disclose as stated in rejection of claim 2 above. As discussed in claim 2, Boerstler discloses wherein each of the N timing signals are coupled to an output of an associated amplifier (Column 2 Lines 51-56, wherein, each of the outputs of the inverter amplifiers is interpreted as each of the N timing signals).

Regarding, each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier. As discussed in claim 2, Gardner et al. discloses, each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier (Column 3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the signal that is coupled to a highest gain amplifier and is not independent of a most significant bit output from said associated amplifier).

Regarding claim 12: Mueller and Gardner et al. as stated in rejection of claim 1 above. Mueller or Gardner et al. do not disclose, wherein N is greater than one, and the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock, however, as discussed in claim 2, Boerstler discloses, wherein N is greater than one, and the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock (Column 2 Lines 51-56, wherein, the integer seven is interpreted as the number of outputs, N, that is greater than one).

12. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller and Gardner et al., and further in view of Eory (US 5,832,043).

Regarding claim 4: Mueller and Gardner et al. as stated in rejection of claim 1 above. Gardner et al. further discloses that the fractional interpolator filter comprises: a shift register having parallel inputs coupled to the N data inputs and to the strobe (Column 24 Lines 54-55). Mueller or Gardner et al. do not disclose, N bit splitters each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined-by the timing signal that is not the MSB.

However, Eory discloses, N bit splitteres each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined by the timing signal that is not the MSB (Column 6 Lines 1-12). It is desirable to have N error-formatters (N bit splitters) in the circuit of Mueller and Gardner et al. A bit splitter allows for the separation and distinction of most significant bits from least significant ones. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include N bit splitters in the circuit of Mueller and Gardner et al., as Eory discloses, in order to distinguish between most significant bits and least significant bits.

Regarding claim 5: Mueller and Gardner et al. as stated in rejection of claim 4 above. Mueller further discloses that the fractional interpolator filter further comprises:
N sub-blocks each having an input coupled to an output of the shift register and an input coupled to an output of an error-formatter (Paragraph 0027 Lines 1-3).
Regarding, coupled to an output of an error-formatter (bit splitter), as discussed in claim 4 above, Eory discloses an error-formatter (Column 6 Lines 1-2).

Regarding claim 6: Mueller and Gardner et al. as stated in rejection of claim 5 above. Mueller further discloses that the sub-blocks are of the type Farrow sub- blocks, linear interpolators, or polynomial interpolators (Paragraph 0032 Lines 1-4).

8. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller in view of Harnden et al. (US Pub 2003/0069009).

Regarding claim 20: Mueller discloses a fractional interpolator having an input coupled to each of the N parallel input streams for interpolating in parallel at least one interpolated data point from the data samples input along each of the N input streams, and N parallel outputs for outputting in parallel the interpolated data points (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2; Examiner notes that N=1); and a numerically controlled oscillator NCO having a plurality of N outputs coupled to respective N inputs of the fractional interpolator for providing N timing signals for respective ones of the interpolated data joints (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4; Examiner notes that N=1); wherein the interpolated data points exhibit an output rate of I/T that is cyclically independent of the sample rate I/Ts (Paragraph 0024 Lines 1-7, wherein, 'Fc' is interpreted to correspond to I/T, and "Fi" to correspond to I/T). Mueller does not disclose means for separating a plurality of at least 2N input data samples into N parallel input streams, the 2N data samples defining a sample rate of 1/Ts.

However, Harnden et al. discloses means for separating a plurality of at least 2N input data samples into N parallel input streams, the 2N data samples defining a sample rate of 1/Ts (Paragraph 0041 Lines 1-6, wherein, "m" interpreted to be 2N and "n" is interpreted to be N). It is clearly obvious to one skilled in the art that a complex signal

must be reproduced at the receiver, using the I and Q components, before interpolation is to be performed on said signal. Reproducing the complex signal using a polyphase filter comprising 2N inputs and N outputs results in much lower delay and greater computational efficiency. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include means for separating a plurality of at least 2N input data samples into N parallel input streams, such as the polyphase filter disclosed by Harnden et al., in the circuit of Mueller, in order to result in an interpolation circuit with lower delay and greater computational efficiency.

Regarding claim 21: Mueller and Harnden et al. disclose as stated in rejection of claim 20 above. Mueller also discloses that the NCO has an input coupled to an output of a timing source that is independent of a timing source used for the input data samples (Paragraph 0028 Lines 1-5).

Allowable Subject Matter

13. Claims 8-9 are allowable if rewritten or amended to overcome the objections.

14. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nader Bolourchi whose telephone number is (571) 272-8064. The examiner can normally be reached on M-F 8:30 to 4:30.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David. C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

David Payne

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER

Nader Bolourchi
7/12/2007
Art Unit 2611